ABSTRACT OF THE DISCLOSURE

Disclosed is a DLL (delay locked loop) circuit for outputting a phase lock signal having a predetermined phase relationship with an input signal. The DLL circuit has: a functional block having a constant-current source; and bias generation means for generating a constant current source bias signal for controlling the constant current source of the functional block, the bias generation means comprising bias control means which changes the bias signal according to the frequency of the input signal.

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